Fig.1.

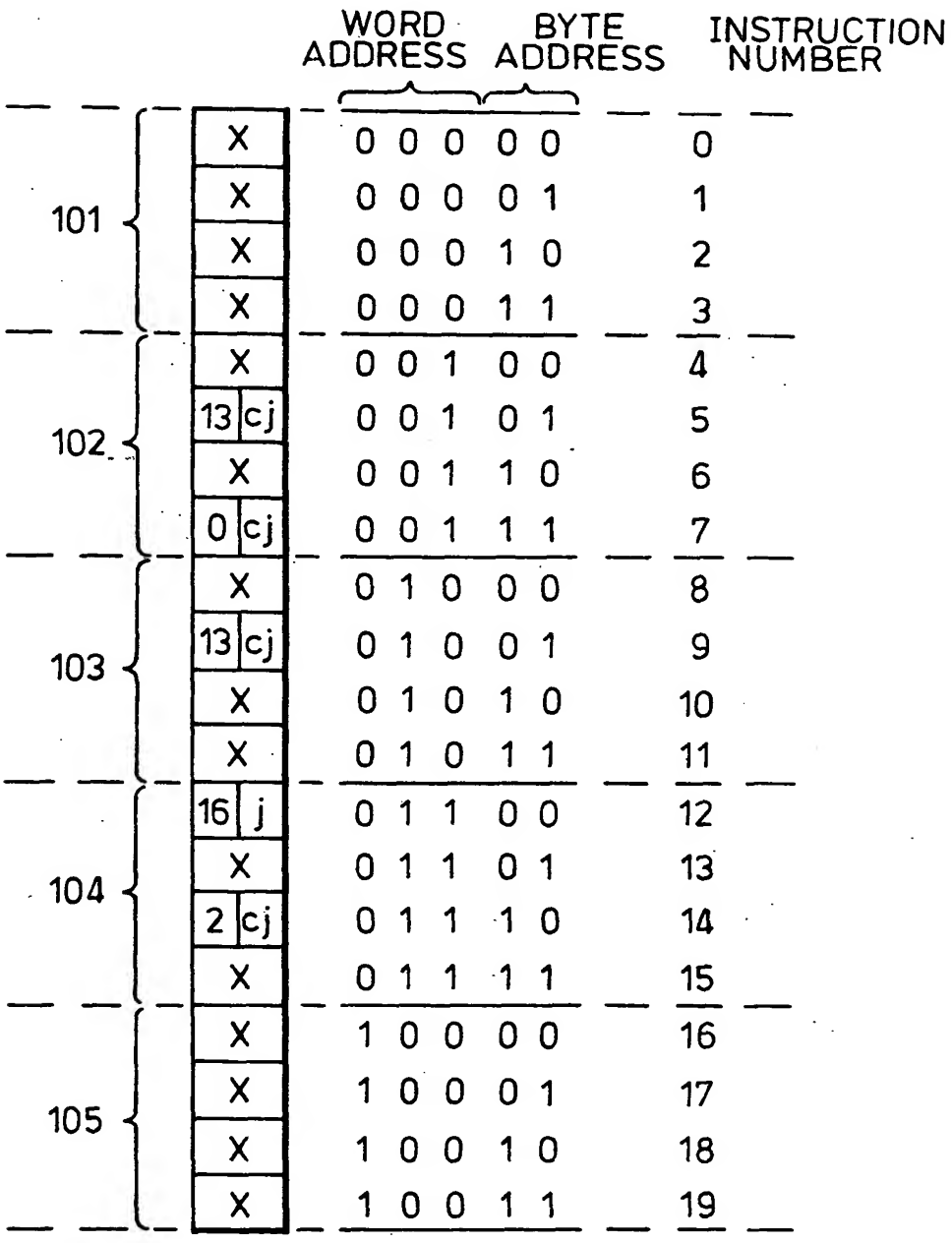

WORD ADDRESS
BYTE ADDRESS
INSTRUCTION NUMBER
101
102
103
104
105
X
13 cj
0 cj
16 j
2 cj
0 0 0 0 0 0
0 0 0 0 1 1
0 0 1 0 0 4
0 0 1 0 1 5
0 0 1 1 0 6
0 0 1 1 1 7
0 1 0 0 0 8
0 1 0 0 1 9
0 1 0 1 0 10
0 1 0 1 1 11
0 1 1 0 0 12
0 1 1 0 1 13
0 1 1 1 0 14
0 1 1 1 1 15
1 0 0 0 0 16
1 0 0 0 1 17
1 0 0 1 0 18
1 0 0 1 1 19

Fig.2.

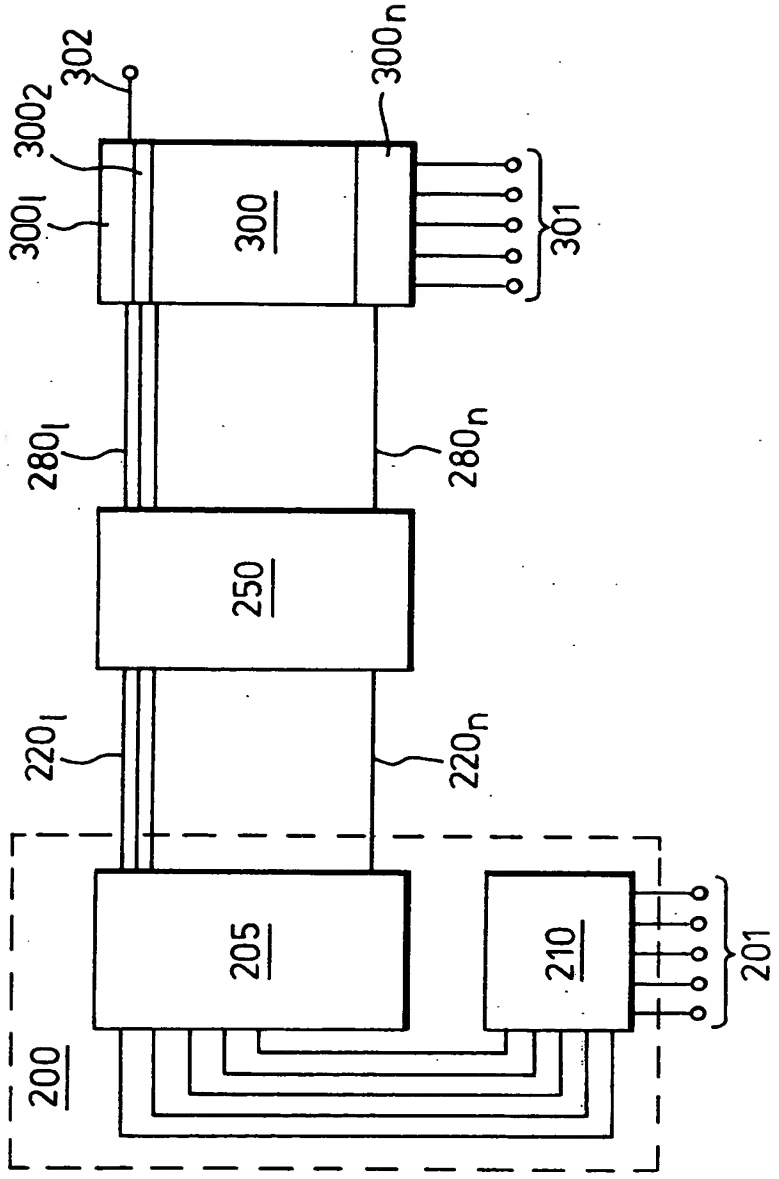

200
205
210
201
250
220₁
220n
280₁
280n
300
301
300₁
3002
302
300n

Fig.3.

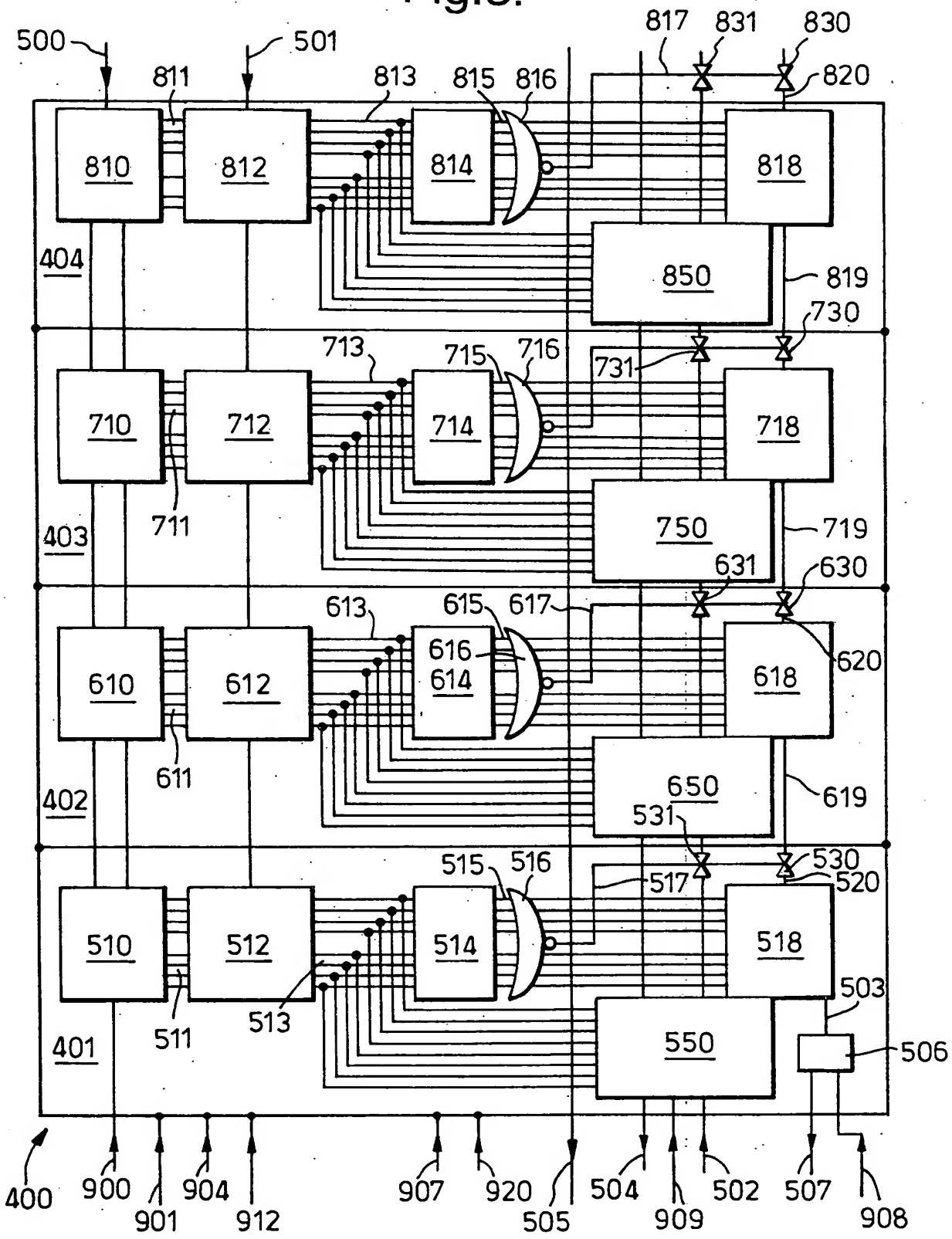

500
501
811
813
815
816
817
831
830
820
810
812
814
818
404
850
819
730
713
715
716
731
710
712
714
718
711
403
750
719
631
630
613
615
617
616
614
620
610
612
618
611
402
650
619
531
530
515
516
517
520
510
512
514
518
503
513
511
401
550
506
400
900
901
904
912
907
920
505
504
909
502
507
908

Fig.4.

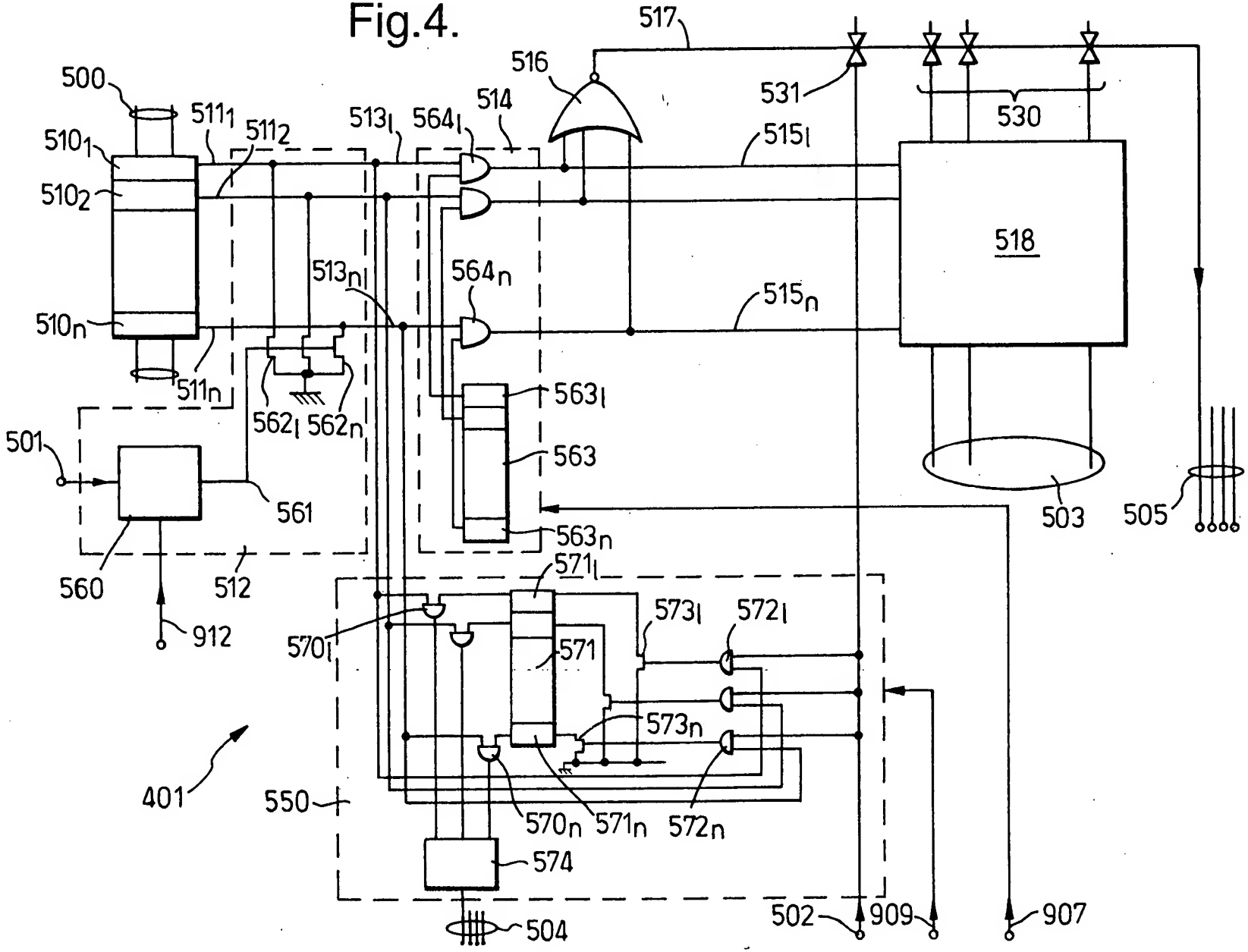

517
516
514
500
511_1
512_1
513_1
564_1
510_1
510_2
510_n
513_n
564_n
511_n
562_1
562_n
501
561
560
512
912
563_1
563
563_n
571_1
570_1
571
573_1
572_1
573_n
401
550
570_n
571_n
572_n
574
504
531
530
515_1
515_n
518
503
505
502
909
907

Fig.5.

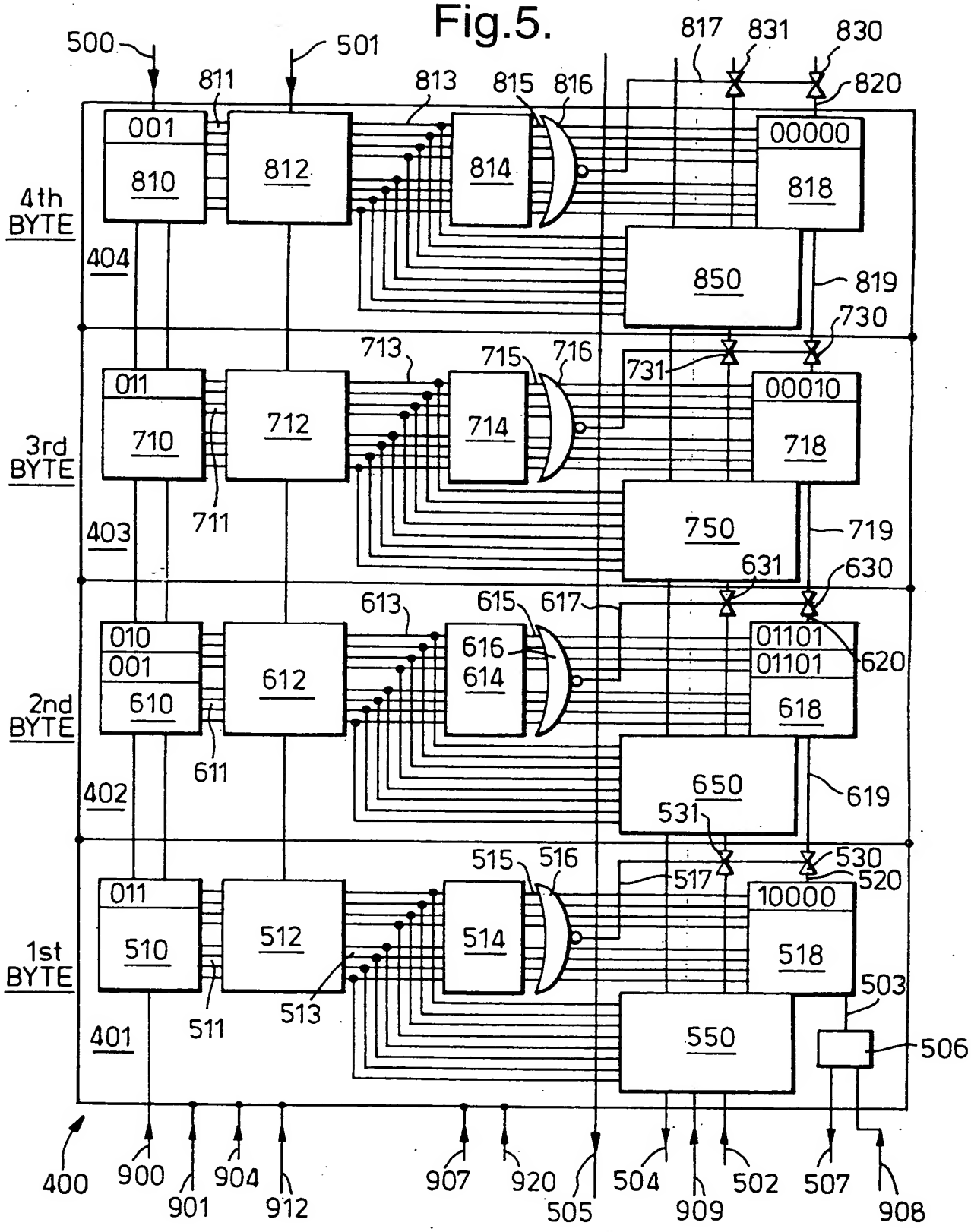

500
501
811
813
815
816
817
831
830
820
001
810
812
814
00000
818
4th BYTE
404
850
819
730
713
715
716
731
011
710
712
714
00010
718
3rd BYTE
711
403
750
719
631
630
613
615
617
010
001
610
612
616
614
01101
01101
620
618
2nd BYTE
611
402
650
619
531
515
516
530
517
520
011
510
512
514
10000
518
1st BYTE
513
503
511
401
550
506
400
900
901
904
912
907
920
505
504
909
502
507
908

Fig.6.

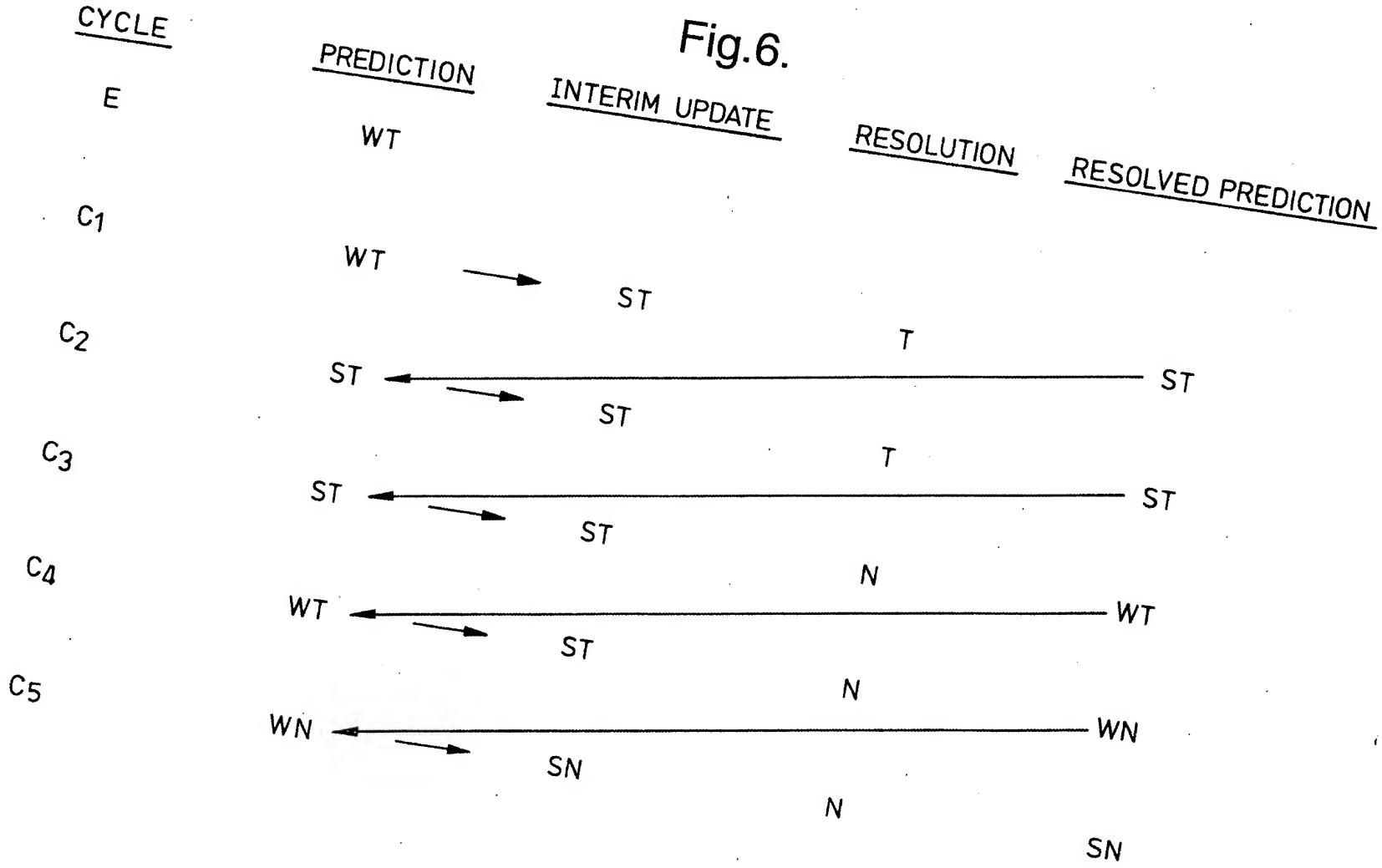

CYCLE
PREDICTION
INTERIM UPDATE
RESOLUTION
RESOLVED PREDICTION
E
WT
C1
WT
ST
C2
T
ST
ST
ST
C3
T
ST
ST
ST
C4
N
WT
ST
WT
C5
N
WN
SN
WN
N
SN

Fig.7.

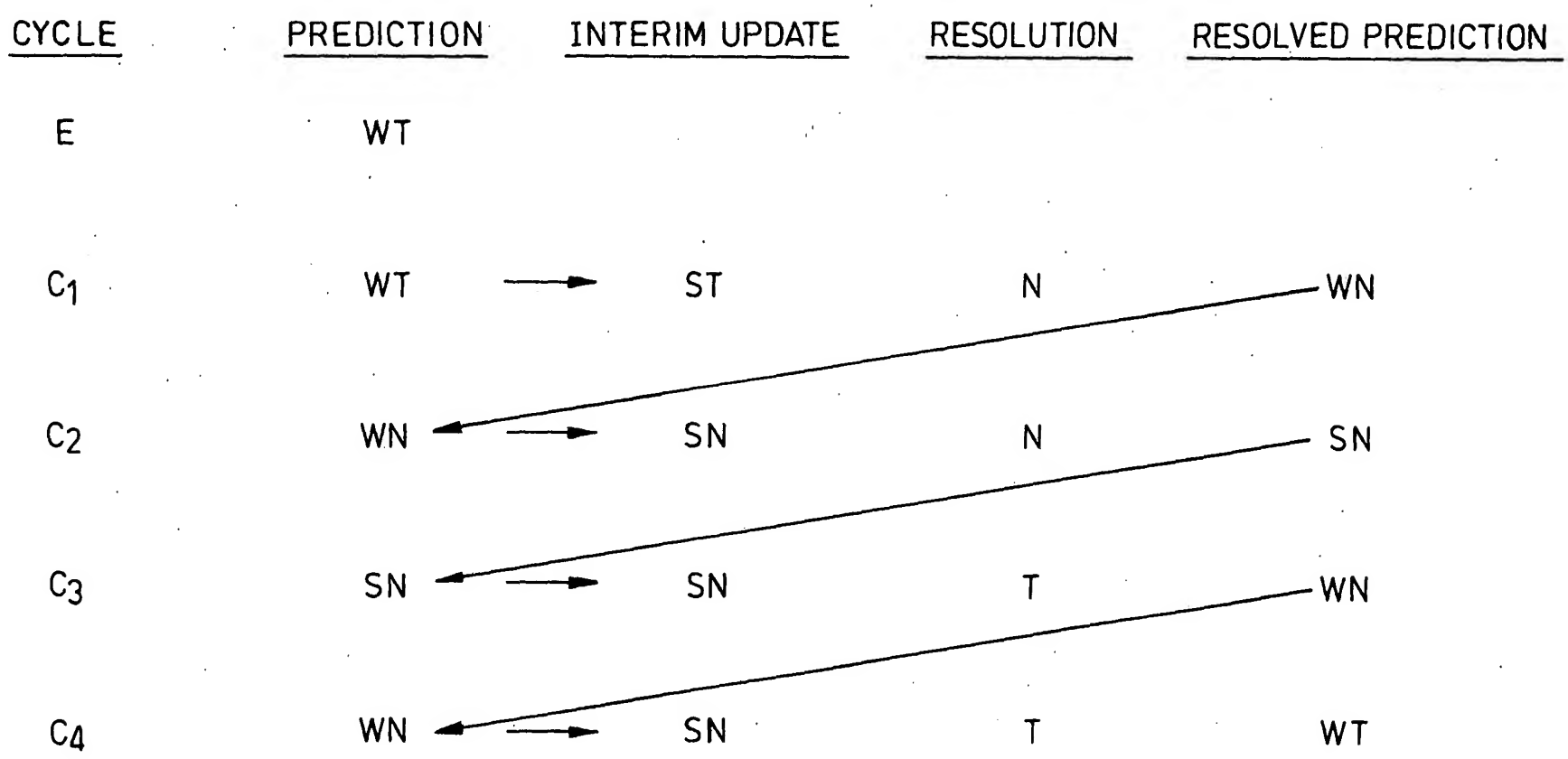

CYCLE
PREDICTION
INTERIM UPDATE
RESOLUTION
RESOLVED PREDICTION
E
WT
C1
WT
ST
N
WN
C2
WN
SN
N
SN
C3
SN
SN
T
WN
C4
WN
SN
T
WT

Fig.8.

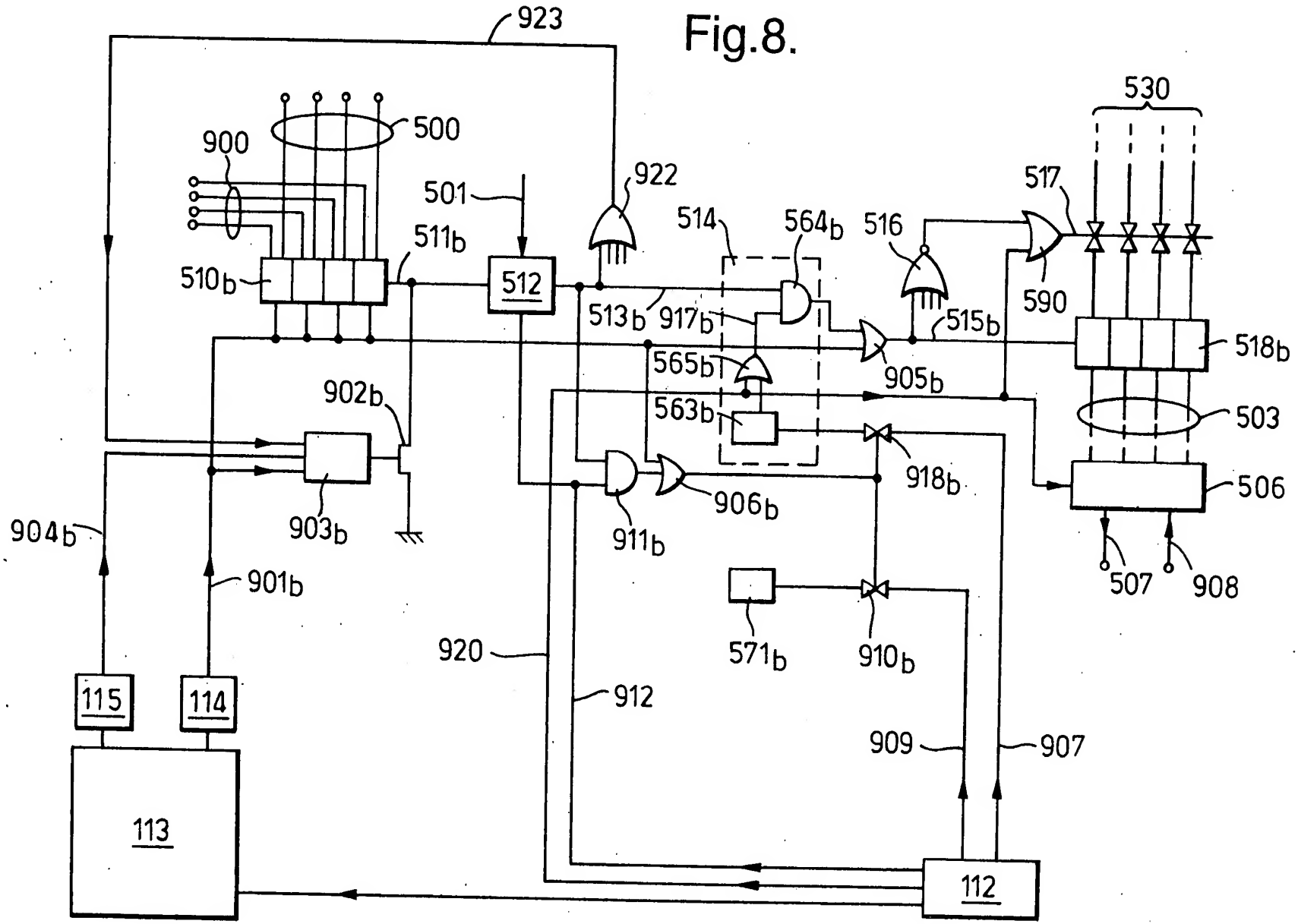
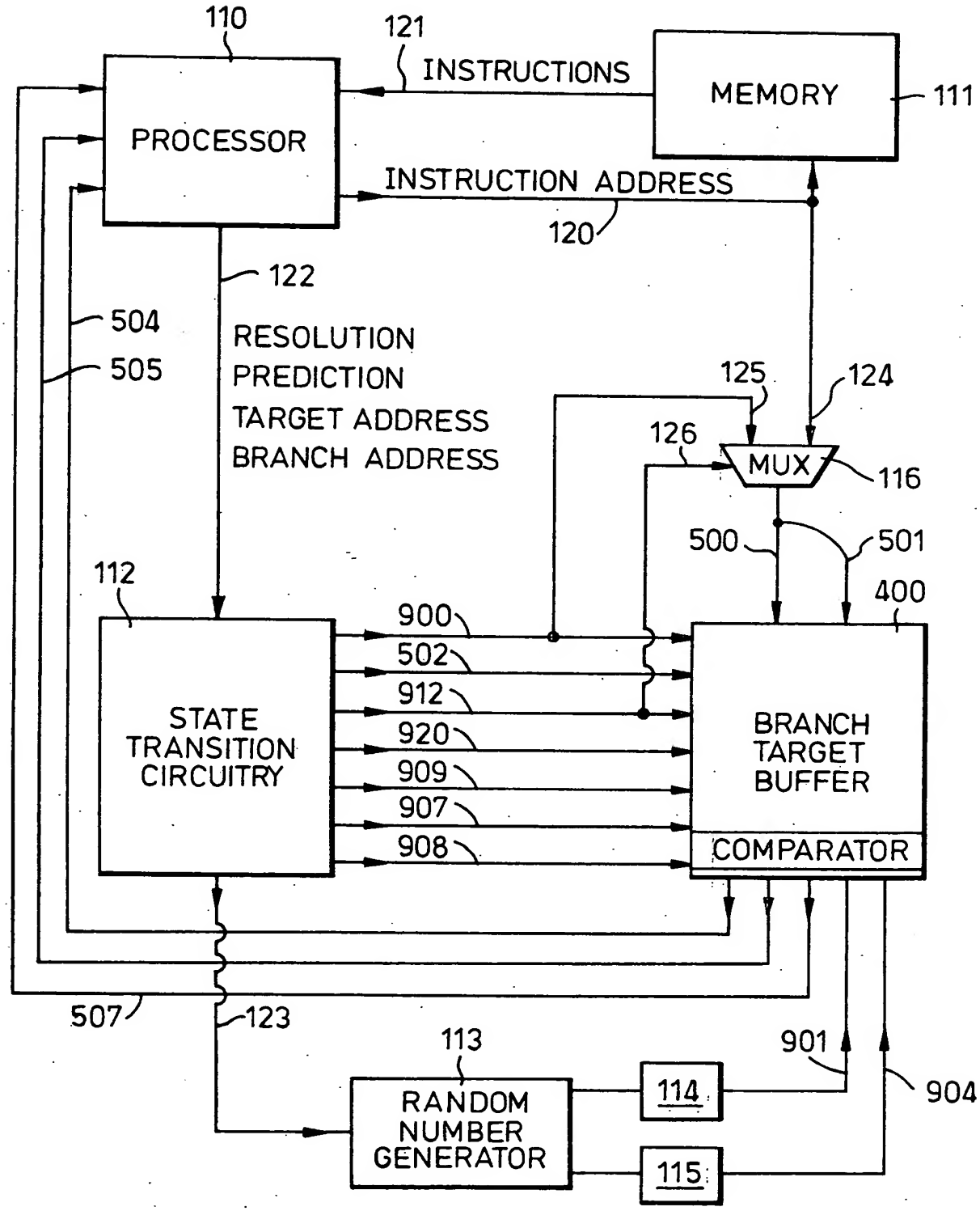

923
900
500
501
922
530
517
514
564b
516
511b
510b
512
513b
917b
590
515b
518b
565b
905b
902b
563b
503
918b
906b
506
904b
903b
911b
907
901b
920
571b
910b
912
115
114
909
113
112

Fig.9.


110
121
INSTRUCTIONS
MEMORY
111
PROCESSOR
INSTRUCTION ADDRESS
120
122
504
505
RESOLUTION
PREDICTION
TARGET ADDRESS
BRANCH ADDRESS
125
124
126
MUX
116
500
501
400
112
900
502
912
920
909
907
908
STATE
TRANSITION
CIRCUITRY
BRANCH
TARGET
BUFFER
COMPARATOR
507
123
113
901
904
RANDOM
NUMBER
GENERATOR
114
115